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DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING, MS 0404
9500 GILMAN DRIVE
LA JOLLA, CA 92093-0404

March 9, 2017

Dear Student Travel Grant Committee Members:

It is my pleasure to write this recommendation for Mohsen Imani's application to the DAC Richard Newton Young Student Fellow Program. I was very happy to be able to attract Mohsen to my group last year as a PhD student. His application, with 25 published papers in the area of circuit and system design, high GPA from a top program in his country, and extremely strong recommendation letters, earned him a rare three year Powell's fellowship at UCSD, one of the most prestigious fellowship offers at UCSD. In CSE department we award only a handful of fellowships every year, with most students getting GSR or TA offers only for the first year. Not surprisingly, Mohsen has continued to be amazingly productive, while earning top grades in his classes (4.0 GPA at UCSD). Just in his first quarter he submitted two conference papers, and has continued at this pace ever since. Exposure to DAC at this early stage in his PhD program would be very helpful to expanding his research horizons. In short, I believe that he is a very deserving candidate for the DAC Student Travel Award.

Before joining my group, Mohsen had worked on Low Power, High Performance, Nanosystem Laboratory where his work was designing ultra-low power and process tolerant digital systems. At the circuit level, Mohsen designed several low power and reliable circuits in subthreshold and nearthreshold regions. He also introduced a new power gating technique for FinFET transistor based systems and proposed a new optimization method based on Simulated Annealing (SA) algorithm. His work resulted in 26 publications, very unusual for a master's level student.

Mohsen research in my System Energy Efficient lab has been focused on circuit and system level memory design. Mohsen's recent paper on "Ultra-Efficient Processing In-Memory for Data Intensive Applications" has been accepted at DAC. He designed an ultra-efficient approximate processing in-memory architecture, called APIM, which exploits the analog characteristics of non-volatile memories to support addition and multiplication inside the crossbar memory, while storing the data. The proposed design eliminates the overhead involved in transferring data to processor by virtually bringing the processor inside memory. APIM dynamically configures the precision of computation for each application in order to tune the level of accuracy during runtime.

Mohsen has also proposed a new SRAM architecture which efficiently exploits FinFET transistors for low-power cache design. He addressed overall design issues that can arise with using FinFET transistor, including cell and cache architecture levels. His new cell improves power consumption and cell variability, while meeting the performance targets of traditional SRAM cache. By

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considering adaptive back-gate feedback and read stability, the proposed cell design provides better characteristics in representing zeros. The results show that the proposed design improves dynamic power, static power, and variability up to 25%, 15% and 52%, respectively, compared to other state-of-the-art cache designs while guaranteeing 2.7X lower NBTI degradation with negligible area overhead. He is currently working on data-aware STT-RAM/SRAM hybrid cache structure. The goal is to ensure the most efficient mapping of data to hybrid cache structure.

Mohsen's impressive research track record, his amazing 4.0 GPA at UCSD, and incredible drive and initiative make him a very deserving candidate for the DAC travel grant. In receiving this grant, Mohsen will gain a strong foundation for his future research. I would be happy to support the rest of his travel costs. If you need more information, please do not hesitate to contact me.

Sincerely,

Prof. Tajana Simunic Rosing