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A new low-power 10T SRAM cell with improved read SNM

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This paper describes the characteristics of a new 10T structure for SRAM cell that works quite well in the sub-threshold region. This new architecture has good characteristics in write and read delay and energy compared with other new structures. This new 10T topology improves read static noise margin (SNM) and write operation speed with respect to other topologies in the same or even lower power consumption. The new topology has at least 13% lower power consumption compared with the best of recent architectures. Its write characteristics also are similar to those of 6T-SRAM, which has improved write delay and energy. The new 10T SRAM cell also consumes lower power compared with other cells. The stacking is used to suppress the standby leakage through the read path. The simulations were performed using HSPICE 2011 in a 16 nm bulk CMOS Berkeley predictive technology model (BPTM).

Keywords: digital electronics; logic; low power circuits; SRAM sell; static noise margin (SNM)

1. Introduction

Currently, designers are concerned about the power reduction of integrated circuits. One effective solution to achieve this purpose is to operate at low supply voltages. Unfortunately, a conventional bulk-based 6T SRAM cell faces several challenges and cannot operate successfully at low supply voltages (Pasandi & Fakhraie, 2013b). By using new technologies, such as FinFET, SOI, 3D designs, nano computing and so on that help mitigate these drawbacks at low supply voltages, is a very attractive area in research but it is very expensive, pushing back the huge investment that exists in the current CMOS technology (Samuel, Balamurugan, Bhuvaneswari, Sharmila, & Padmapriya, 2013). Thus, this necessitates proposing new structures for SRAM cells that are based on traditional technologies and can also address the disadvantages at low supply voltages.

Static power dissipation increases rapidly in new designs (Gupta, Raychowdhury, & Roy, 2010). In present devices, sub-threshold current is the most important part of the static current (Rabaey, 2009). Power gating method is a popular method used for decreasing static power. This method is widely used to decrease leakage of circuits in standby mode. Several optimised and efficient versions of this method have been introduced in numerous papers (Pakbaznia & Pedram, 2012; Pilo et al., 2013; Wang, Ohta, Ishii, Usami, & Amano, 2012). This technique is also implemented in RAMs with CMOS and other transistors (Ohsawa et al., 2012). A good solution to leverage the voltage scaling is operating in a sub-threshold region in analogue (Lee, Lu, & Huang, 2012; Magnelli, Crupi, Corsonello, Pace, & Iannaccone, 2011) and digital circuits (Fuketa, Harada, Hashimoto, & Onoye, 2013; Kumar, Hussain, & Paul, 2013; Lutkemeier

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et al., 2013). Reducing memory parts of processors is very important since the maximum area and power of a sample IC are dedicated to memory such as SRAM, which usually operate with static power consumption (Pasandi & Fakhraie, 2013a). Lowering the supply voltage in this area improves the total energy consumption of the processor greatly.

Recent researches on reducing the power of SRAM apply dynamic voltage scaling (DVS) mostly on an idle block using lowering (Bhavnagarwala et al., 2004; Kanda, Miyazaki, Sik, Kawaguchi, & Sakurai, 2002; Kim, Flautner, Blaauw, & Mudge, 2004; Qin, Cao, Markovic, Vladimirescu, & Rabaey, 2004) and raising ground (Bhavnagarwala et al., 2004; Kanda et al., 2002; Osada, Saitoh, Ibe, & Ishibashi, 2003; Yamauchi, Iwata, Akamatsu, & Matsuzawa, 1996) or simultaneously (Enomoto, Oka, & Shikano, 2003). Moreover, in new technologies scaling the transistors' dimension and supply voltage in memories degrades the stability of the cells. Thus, designs should have high static noise margin (SNM) for being robust against environment noise (Li, Wang, & Kim, 2012; Pilo et al., 2012). In this paper we propose a new 10T SRAM cell that can operate successfully in the sub-threshold region, and thus can have the potential of reducing power consumption. The new design also reduces the leakage current through the read path, which can lead to integrating more cells sharing the same bit line (BL) in the SRAM array. This can help reduce the power and area of SRAM by sharing the peripherals used for each column in an SRAM array.

The rest of the paper is organised as follows. Section 2 describes different components of leakage current in CMOS transistors. Section 3 reviews several architectures for SRAM cell in recently published papers. In Section 4, the proposed architecture for SRAM cell is discussed. In Section 5, characterisation of the proposed SRAM cell is presented. Finally, Section 6 concludes the manuscript.

2. CMOS leakage analysis

As Figure 1 shows, there are five dominant leakage sources in short channel transistors: sub-threshold leakage, gate-induced drain leakage (GIDL), punch-through, junction leakage and gate leakage (Rabaey, 2009).

2.1. *Reverse p-n junction leakage*

The two reverse p-n junction currents J_{SB} and J_{DB} flow between drain and source of the transistor and the substrate. This current consists of drift/diffusion of minority carrier in depletion regions and electron-hole generation.

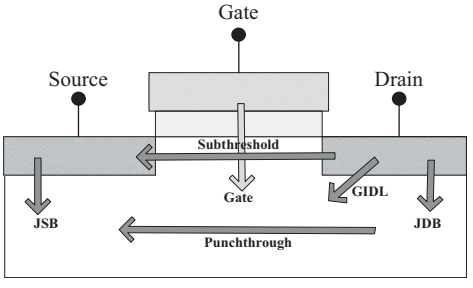

Figure 1. Leakage source in short channel devices.

2.2. *Tunnelling through gate oxide*

The gate oxide leakage of new MOSFET consists of two major tunnelling currents: Fowler–Nordheim tunnelling (FNT) and direct tunnelling (DT). FNT is reduced very much in nano meter devices because of scaling the voltage in ultra-low power design that works in the sub-threshold operation region of MOSFET. FNT current through the gate oxide is related to the field applied to the gate oxide as shown by Equation (1). The low field across the gate oxide due to DVS is not enough for FNT current in the sub-threshold region, so this portion of gate leakage is suppressed in sub-threshold designs.

$$J = AE_{ox}exp\left(\frac{-B}{E_{ox}}\right) \tag{1}$$

The other portion of gate oxide leakage consists of DT of carriers through the gate oxides as thin as 3 nm. This portion of gate leakage is not as destructive as FNT for devices but can increase the leakage from the gate and degrade the integrated circuit in the view of temperature instability and power consumption. New methods are utilised, which omit DT through the gate oxide such as thick gate oxide using high-K materials and so on, and thus this is not much of a concern in the latest designs (Wilk, Verghese, Chen, & Maes, 2013).

2.3. *Sub-threshold leakage*

This part of leakage that is dominant in current design comes into forefront in the sub-threshold region of a transistor where the gate voltage is below the threshold voltage. The current is exponentially related to voltage in this region because of dominant diffusion current through the drain junction. This relation is such as shown in Equation (2) (Elmasry et al., 1995):

$$I_{Dsub} = I_0 exp\left(\frac{V_{GS} - V_T - \eta V_{DS}}{\eta V_{th}}\right)\left(1 - exp\left(-\frac{V_{DS}}{V_{th}}\right)\right) \tag{2}$$

The reduction of threshold voltage of the transistor due to day-by-day scaling of devices results in an exponential increase in static leakage. This component of leakage is major in off state when V_G is zero, especially in scaled devices below 65 nm, which can be shown by Equation (2). This component of leakage current dominates the current technology, where all other elements are omitted by new approaches. This paper focuses on reducing the sub-threshold leakage current of SRAM by deforming the access transistor topology.

3. SRAM cell topologies

Some of the main problems of SRAM cells in the strong region when the supply voltage is scaled down are read failure, write failure and low SNM. A conventional 6T-SRAM is demonstrated in Figure 2, which has the same path for write and read operations. This cell is not good candidate for low power design, since it has stability problems in this region.

There are several designs that try to compensate the performance issue of the cell when operating at very low supply voltages. These architectures try to achieve the power objectives in the design while maintaining the performance. Read and write SNM should be kept at a balanced rate when the device is operating in a supply voltage of about 300 mV. Schmitt-trigger-based SRAM cell (ST10T) (Kulkarni, Kim, & Roy, 2007) and

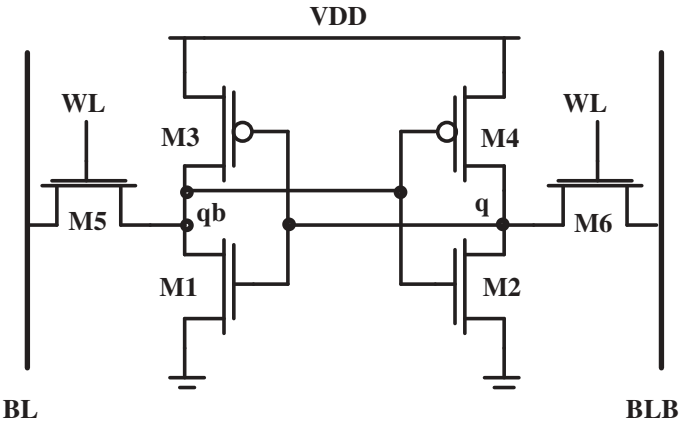

Figure 2. Conventional 6T-SRAM cell (Weste & Harris, 2011).

LP10T (Islam & Hasan, 2012) cells are two powerful topologies in strong inversion region. ST10Ts topology is depicted in Figure 3 and the LP10T structure is shown in Figure 4. Both are employed to operate as a SRAM cell in strong inversion regions with the improvement of reduced power.

The main problem of the ST10T cell is its stability parameters due to weakening of the cell in all operating modes (due to stacked transistors in the cell). The second structure, LP10T, on the other hand, proposed an innovative approach so as to be able to reduce leakage current in its idle time. The virtual ground (VGND) in the bottom of the back-to-back inverters makes it possible to increase the level of the local ground in some inactive cells in order to decrease the pernicious leakage. This is controlled via a logic circuit so as to be able to write and read from any row and column of the cells. Increasing the ground voltage can easily weaken the inverters besides affecting its power. Thus, in the reading

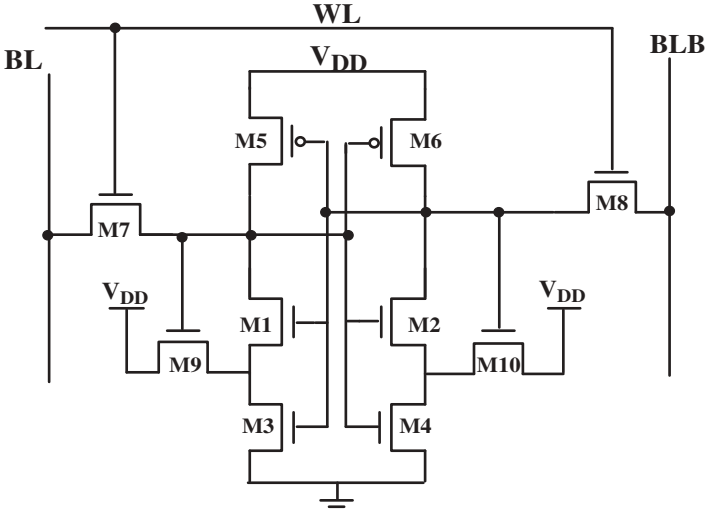

Figure 3. Schmitt trigger-based 10T SRAM cell (ST10T) (Kulkarni et al., 2007).

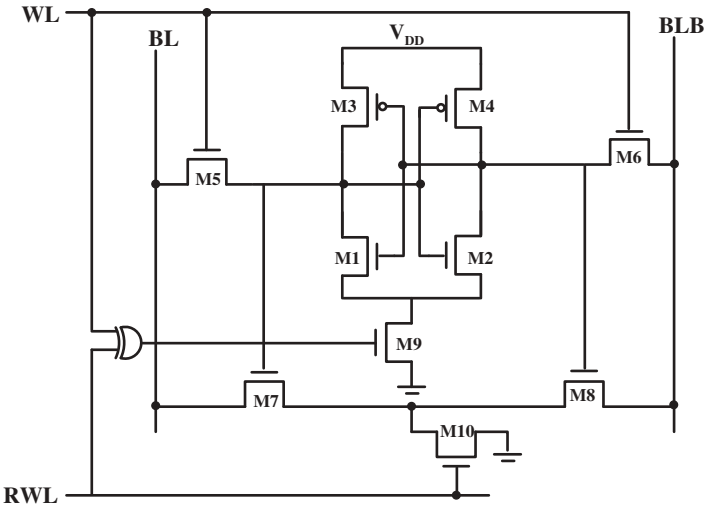

Figure 4. LP10T architecture (Islam & Hasan, 2012).

mode, voltage of the cell can be disturbed when it is unbiased and has a VGND higher than zero. Although the controller can cautiously decrease the ground voltage during the write operation, it is also possible for the cell to be disturbed during the hold phase. In other words, noise form external sources can easily affect the cells and decrease the hold stability of the cell.

4. Proposed architecture

The proposed architecture of the ultra-low-power SRAM is demonstrated in Figure 5. In contrast to SRAM cells such as those described in Chang, Kim, Park, & Roy (2009), there are two transistors in the write path; however, in our proposed design there is just one transistor in the write path. Write and read access transistors for the proposed cell are individual. M5 and M6 are write access transistors and M7–M9 are for read access.

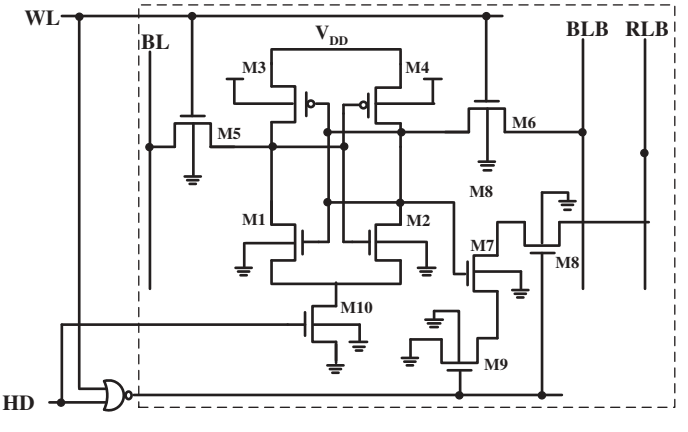

Figure 5. Proposed SRAM cell with buffered read access path.
Note: HD, hold signal.

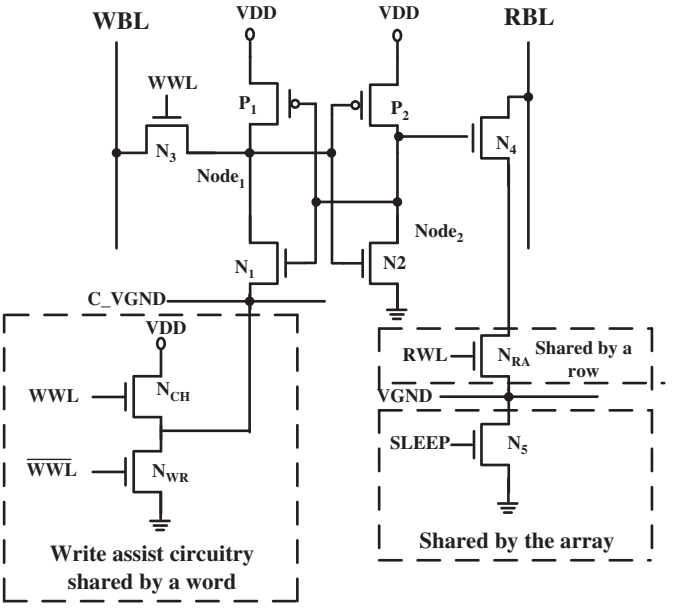

Figure 6. Power gated 6T SRAM cell presented in Jiao and Kursun (2010).

Having individual access transistors allows their sizing individually. This will lead to increase write-ability and read stability of the cell by eliminating the sizing conflict of access transistors for conventional 6T-SRAM cells (Weste & Harris, 2011).

In the SRAM cell described by Jiao and Kursun (2010) (Figure 6), there are three transistors in the read path between read BL and ground. One of these transistors is common for all cells in the array and will be OFF just in idle modes to reduce the leakage current. So, in the read mode there will be one or two OFF transistors (depending on the voltage of the left internal node of the cell). Thus, leakage current through read path (flows from read BL to the ground) is similar to conventional 6T SRAM cells in half of the states. In the SRAM cell described by Jiao and Kursun (2010), one of the three stacked transistors in the read path is common for all cells in the same row; however, sharing this transistor can reduce the number of transistors used in each cell, which leads to saving some area, but this has a problem. As depicted in Figure 7, for SRAM of Jiao and Kursun (2010), there is a possible state that the charge on RBL-1 BL might be discharged falsely due to the shown sneaky current. This will lead to read errors. In the proposed 10T cell, there are three stacked transistors in the read path, and none of them are shared with other cells; thus the discussed sneaky current doesn't exist in the read path. In the proposed cell, there are two or three OFF transistors in the path between read BL and ground for non-selected cells. Thus, I_{on}/I_{off} for the proposed cell will be larger than the conventional SRAM cell and also the SRAM cell discussed in Jiao and Kursun (2010). Having a larger I_{on}/I_{off}, it is possible to integrate more cells sharing the same bit-line. Thus, write and read peripherals of each column in the SRAM array can be shared for more cells. This means that more area and power can be saved. However, in the proposed 10T SRAM cell, the discussed sneaky current is mitigated compared to that in Jiao and Kursun (2010); however, by making three transistors in the read access path individual for each cell, the area of our SRAM cell is increased.

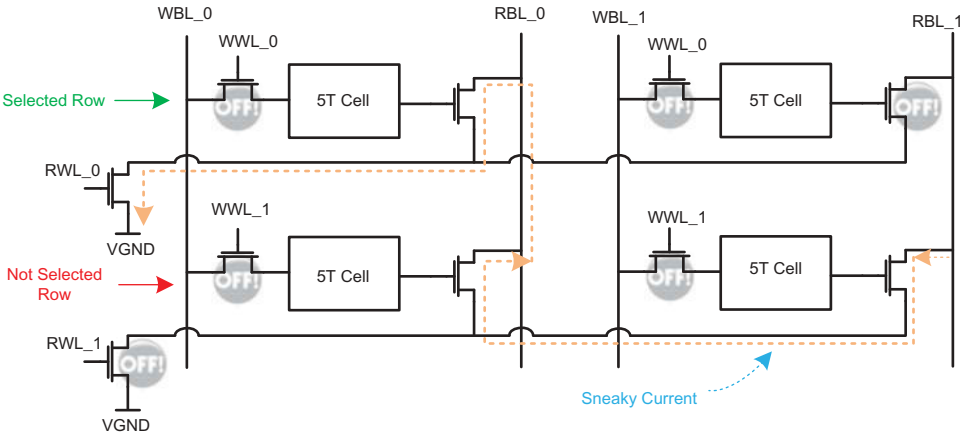

Figure 7. A possible state that can discharge RBL-1 BL falsely.

The back-to-back inverters can consume a lot of power in the holding mode when none of read or write operations are being carried out. This high power consumption can be decreased by weakening the inverters utilising the stacking effect. This was performed by adding a transistor (M10) to the tail of the storage loop. This transistor is kept OFF in the holding mode, which results in ultra-low-power consumption. However, when the cell is being read or written, the transistor goes to the saturation region by HD control signal. The added transistor also drops some voltage by itself (overdrive voltage of M10), which weakens the cell in write operation and will increase the write-ability of the cell. The read operation can be performed more easily with higher SNM by keeping the M10 in the ON mode strongly.

The proposed architecture is a powerful design in low-voltage operation. A powerful buffer in the write and read paths can guarantee down to 130 mV operation by correct read and write operations with respect to other techniques. The convectional 6T-SRAM is stable by the supply voltages higher than 300 mV, which is very high in the new low-power designs. The gate voltage of the M10 transistor is increased and the drain voltage is observed in response to this sweep of gate-source voltage. The drain voltage of M10 is lowered down by sweeping its gate voltage and starting to fall to the ground. It never reaches zero due to the over-drive voltage of M10. It saturates the lowest value of voltage in the VGND. The change in this voltage is depicted versus time in Figure 8. The SRAM cells are used to build an array of memory cells served as catch structures. They need peripherals such as decoders, control signal attributers, input and output buffer and control signal buffers. These components are shown in Figure 9.

5. Characteristic of the proposed SRAM cell

The proposed architecture for the SRAM cell is compared to other recent designs of SRAM based on characteristics such as write access time, power dissipation and SNM. Conventional 6T, Schmitt–Trigger-based 10T (ST10T) (Kulkarni et al., 2007) and low-power 10T (LP10T) (Islam & Hasan, 2012) are compared with the proposed cell in view of all the characteristics mentioned before. The proposed architecture and all of the other architectures are designed using the 16 nm Predictive Technology Model (PTM).

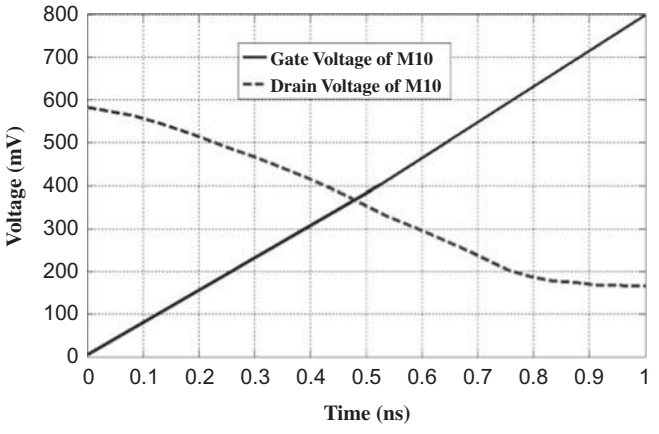

Figure 8. Change in the VGND node in the operating cells.

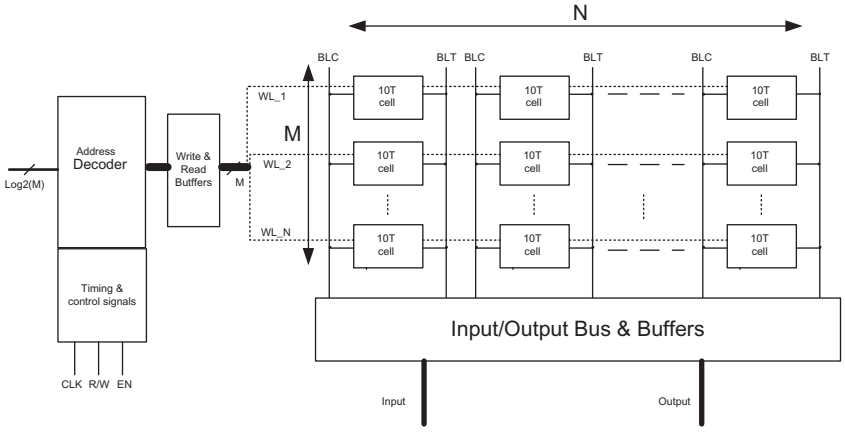

Figure 9. Employing the proposed 10T SRAM by its peripheral to communicate with the CPU.

Read SNM is a quite sensitive characteristic that is damaged by reducing the supply voltage to the sub-threshold region. The voltage of Q node in Figure 2 is higher than zero in read operation, which is due to BLs voltage division between access transistor (M5) and pull-down transistor (M3). This voltage is called Vread. If this voltage is higher than the threshold voltage of the left-hand inverter, the cell flips and read error occurs. The read SNM value is very low for 6T-SRAM. In proposed design this value is improved by buffering the storage nodes from BLs. Figure 10 shows the butterfly in read mode for 6T-SRAM and the proposed SRAM cell at a supply voltage of 0.8 V. As seen, read SNM for our design is better by 2.8 times.

Having large read SNM, it is possible for SRAM cell to operate correctly in the sub-threshold region. Applying Monte Carlo simulation in three different regions shows the applicability of the proposed architecture in the whole spectrum of the voltage even though the operating region of the transistor changes.

The read SNM of the proposed architecture versus supply voltage is depicted in Figure 11 and its variation with respect to temperature is plotted in Figure 12. An

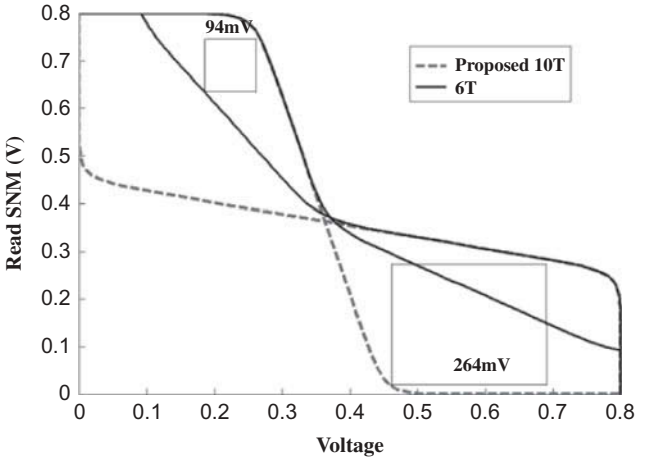

Figure 10. Comparison of the read SNM between 6T and proposed 10T structure in strong inversion region.

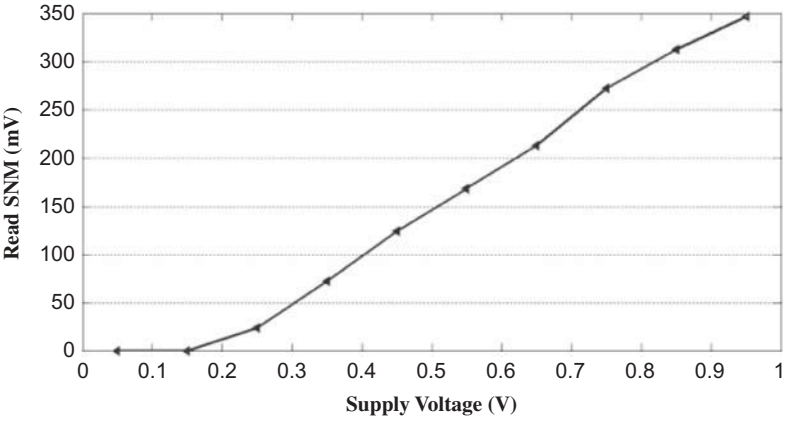

Figure 11. The variability of the SNM for the proposed architecture versus supply voltage.

appealing feature of the proposed architecture is its stability through different values of the Vdd due to buffer stage in the read path. This can reduce the leakage through the read path by two levels of stacked transistors. The cell has a higher strength so as not to be discharged by the read transistors during the read operation. The variability of the read SNM versus temperature is illustrated in Figure 12. This cell has very low SNM variation when faced with a high range of temperatures due to stabilising of the transistors in the read path in different temperatures. In other words, the two series transistors have a lower tendency to change their current and voltage characteristics in different temperatures. The variability of write power versus supply voltage is depicted in Figure 13.

The write access time of the proposed architecture is improved similar to that of the LP10T architecture because of charging of the VGND node, which can weaken the loop. It results in the BLs having more control in the inverters loop.

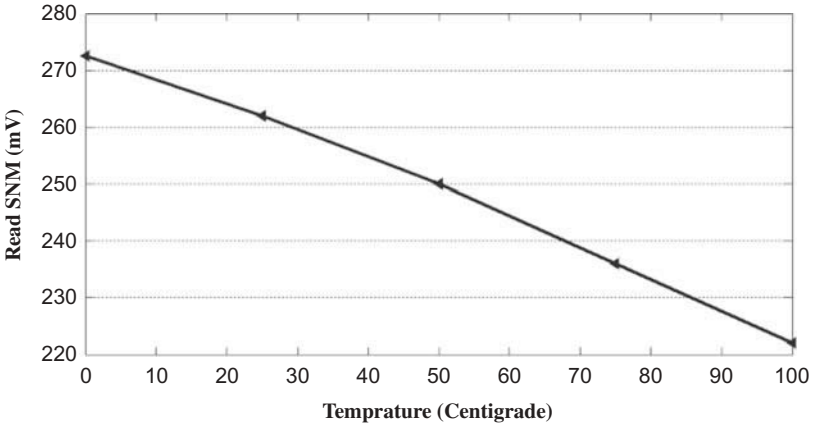

Figure 12. The variability of the SNM for the proposed architecture versus temperature.

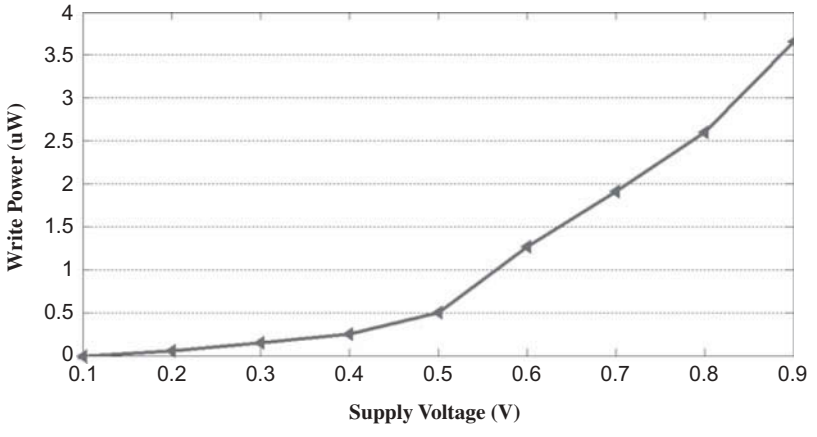

Figure 13. The variability of the write power for the proposed architecture versus supply voltage.

The write access times are measured between 10% change of the initial value of the desired nodes until it reaches its final value by a 10% margin. The SNM and write delay times and its variability of structures are archived in Table 1. The supply voltage was assumed as 0.7 V. Figure 14 shows the comparison of standby power in LP10T and the

Table 1. Comparison of the read SNM, write delay and hold power for different designs.

		Write delay		
Cell	Read SNM (mV)	Value (ps)	Variability	Hold power (nW)
6T	57.9	70.81	0.05	24.9
ST10T	208.5	77.54	0.06	15.1
LP10T	220.4	76.02	0.05	6.4
Proposed 10T	225.1	73.28	0.05	6.1

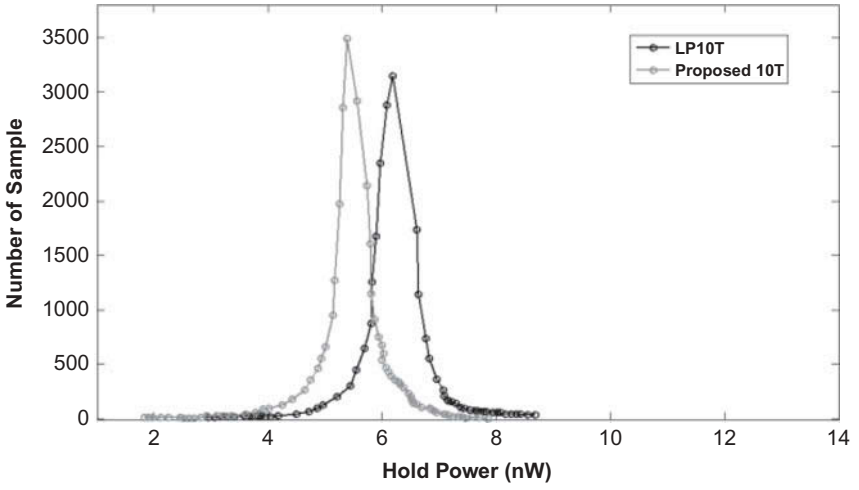

Figure 14. Comparison of hold power of LP10T and the proposed structure in 0.8 V.

proposed architecture. The LP10T architecture is one of the optimal power consumption structures among the new introduced cells. As it is shown, the proposed architecture has a better result than LP10T.

The lower write time in this architecture, which is achieved by weakening the SRAM cell, reduces the access time of the cell efficiently. The power reduction in this new cell is considerable compared with the recent LP10T cell, which is shown in Figure 14. It shows that the proposed cell reduced the power consumption by more than 45% in different process corners respect to other design.

The layout of the proposed cell is depicted in Figure 15. In this figure, we assumed that the tail transistor (M10 in Figure 5) is shared among 32 cells (corresponding to bits of a 32-bit word) in the SRAM array. The node virGND in the layout of the proposed cell refers to this shared rail. Thus, by choosing W/L of this tail transistor to be 32 times larger than the minimum size ($W/L = 64$ for $L = L_{min}$), the proposed SRAM cell consumes 47% more area compared to the 6T-SRAM cell. According to area comparisons mentioned in Islam and Hasan (2012), area of our cell is smaller than the cells used in Islam and Hasan (2012) and Kulkarni et al. (2007) by 44% and 74%, respectively.

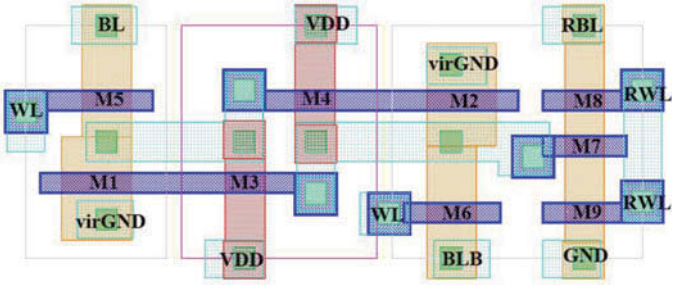

Figure 15. Layout of the proposed SRAM cell.

6. Conclusion

The proposed SRAM cell for read operation has ultra-low static power. The main characteristic of this method is its feasibility to be operated in high frequency due to improved drive current and safe operability in the sub-threshold region. Its well-developed structure has the tendency of reducing power and write time of the SRAM cells. The recent topologies of low-power SRAM cell are compared to the developed architecture and their power penalty and their lack of stability are investigated with respect to the proposed architecture. More than 13% reduction in the same area and same access time is its appealing characteristic. The stability of the proposed architecture in the sub-threshold region is of special interest to current IC designs.

Disclosure statement

No potential conflict of interest was reported by the authors.

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