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Ultra-low power FinFET based SRAM cell employing sharing current concept

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ABSTRACT

This paper proposes a new ultra-low leakage, single-ended FinFET-based SRAM cell to improve the stability and read ON/OFF current ratio. The design employs a power gate transistor that shares the read path and main body current to improve the cell stability (SNM) by reforming the butterfly curves. In addition adjusting the tail transistor strength reduces the hold power, suppresses the variability of the cell by acting as internal feedback and improves write ability in active mode by decreasing the voltage drop over the cell. The proposed architecture redesigns the read path circuit and leverages voltage boosting for biasing, effectively eliminating access transistor leakage in read, write and hold modes. With 20 nm FinFET technology, the results show that in above threshold (near threshold) region, the proposed structure has at least 2.2× (3.5×) lower static power, with 15% (16%) lower static power variation with respect to other state-of-the-art 10T cells. Additionally, our results show that the proposed cell improves the ON/OFF current ratio by at least 20× and 6.5× compared to prior designs in above threshold and near threshold regions respectively.

1. Introduction

Scaling of conventional CMOS technology has been motivated by the need for higher integration density and performance over the last few decades. Static power consumption is a major concern when designing nano-scaled integrated circuits, due to the exponential dependence of subthreshold current on the threshold voltage V_t. Embedded SRAM comprises a dominant portion of chip area, and the power consumption in modern SoCs. In SRAM cells, where the contents must be retained for long durations with a constant power supply, the subthreshold current is a significant source of power consumption. Therefore, when designing future SRAM cells for low-power applications, a vital design objective is to minimize the subthreshold current.

Circuit design techniques devised to reduce the static power of SRAM blocks include lowering the supply voltage [1–3], raising ground [4], or using both techniques simultaneously [3,5]. In subthreshold regions, power reduces considerably, but the performance penalty is severe. Alternatively, near-threshold computing (NTC) is a region of interest in new ultra low power and high performance designs, where supply voltage is near the threshold voltage of the transistors [6].

Several efforts explore the use of FinFET transistors for low-power SRAM designs [7,8]. FinFETs are good candidates for low supply voltage because of their sharp subthreshold slope, low power consumption and subthreshold leakage. These devices increase the controllability of gate on channel with respect to CMOS transistors and suppress Short Channel Effect (SCE) [8]. However, emerging technologies alone do not satisfactorily address the static power and stability concerns. Even with FinFETs, the main challenge of SRAM at sub-threshold and near-threshold operating points is the stability during read operation, which has not been adequately solved. At low supply voltages, SRAM cells have low stability due to low signal to noise margin and high read path leakage. This situation worsens with high process variations in nano-scale technologies.

In this paper, we address some of these challenges of SRAM cells at low supply voltages.

- To the best of our knowledge, this is the first SRAM cell design that shares the read path and main body current to improve the cell stability (SNM) by reforming the butterfly curves. Sharing the virtual ground between main body and read path ground improves area efficiency, decreases the effective voltage over the cell, and enhances the cell write characteristics. This technique independent of technology type (FinFET, CMOS, etc.) provides inner feedbacks to the cell and decreases the cell variability. The results show that static power reduces by 2.2× and 2.6× with at least 15% lower variability at above and near threshold supply voltages respectively.
- We used the back gate of FinFET device to minimize read path leakage current and improve ON/OFF ratio. Using voltage boosting as read path supply voltage, and by redesigning read path transistor circuit, we reduce the read access transistor leakage in read, write and hold modes. Our results show that the proposed cell improves ON/OFF current ratio by at least 20× and 6.5× compared to other cells at above and near threshold respectively.

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The paper is organized as follows. Section 2 describes background and related work. Section 3 presents the proposed SRAM cell. Section 4 shows simulation results and compares them with other cells. Section 5 concludes the article.

2. Background & related work

2.1. FinFET device

Fig. 1 shows two types of FinFET structures: Independent-gate (IG-FinFET) and Common-gate (CG-FinFET). The fin shape of gate allows higher controllability over the channel and better subthreshold slope compared to CMOS transistors. In the independent-gate device, the back-gate and front-gate fins are separated, while both gates are connected and biased with single voltage in CG-gate device for simpler biasing. The parameters of 20 nm FinFET device are shown in Fig. 1 [9,10]. We identify two main approaches in related work that enhance read stability and reduce power: (i) The use of extra transistors [11–13] and (ii) use of new technologies such as FinFET [14,15]. Note that in this paper, we use the term *leakage current* to denote the drain-to-source leakage current of the transistor when it is in the OFF mode.

2.2. Read enhancement techniques

An SRAM cell is commonly designed as a 6T structure. Since this cell uses the same path for read and write operations, most failures in SRAM cells occur due to issues in read mode. Utilizing different buffers in read mode is an effective method to improve the read operation [11]. With separate read and write access transistors, the read operation is performed with the gate of read path transistor. This decreases the leakage of read path through the main loop and the read Static–Noise Margin (SNM) approaches hold SNM. But this creates a low read I_{ON}/I_{OFF} ratio (ON/OFF current ratio). Cells described in [2,16,17] use a different buffer transistor in read path to improve ON/OFF current ratio.

In *10TCell-1* [2], the main cell body is similar to the conventional 6T SRAM cell. This is a single-ended cell, i.e. the cell value can be read from one side of the cell. In reading zero, read current discharges Read Bit Line (RBL) by passing current through two stack transistors. During read one, high drain–source voltage drops across read access transistor and causes high leakage current (OFF current). To address this problem, *10TCell-2* [16] modified the cell structure such that during read one, one P-type transistor charges intermediate node and creates zero voltage across drain–source of access transistors. *10TCell-3* [17] is slightly different than 10TCell-2 in that it only uses one buffer in read path reducing RBL leakage, and two access P-type and N-type transistors in parallel to improve the switching performance and active current. Although, 10TCell-2 and 10TCell-3 reduce OFF current, this improvement disturbs other characteristics. The access transistors are in active mode and even slight difference between RBL and intermediate node voltage (the source–drain of access transistor) can create high leakage current through read bitline. This leakage becomes significantly high at supply voltages higher than sub-threshold. The other problem in these designs is their RBL leakage during write mode. This current is important because it can alter the value of intermediate nodes and create loop current in cells allocated in the same RBL, and even the cells that use the same Read Word Line signal (RWL). Thus, none of the above methods eliminate leakage current of RBL simultaneously in read, write and hold modes, which is fundamental for power reduction and read stability.

2.3. FinFET based cells

In FinFET based SRAM cells, the back gate of FinFET has been used to control the read performance and write ability of cell [18]. In Ying-Yang feedback cell, the back gate of access transistors is grounded to make them weak [19]. This improves the read stability of cell at the expense of write performance. In [7], the storage node is connected directly to the back gate of access transistor, which improves the write ability and write performance. [20] uses double word line, Write Word Line (WWL) and Read Word Line (RWL), for front and back gates of access transistors respectively. During write operation both lines are activated, while in read mode, only RWL is activated. This method improves read stability of cell. Combining different internal back gate feedback is considered in Schmitt trigger 10T cell [21] to improve the read and write performance. In contrast, our paper considers the effect of back gate feedback, to decrease read path leakage, improve ON/OFF current ratio and all read and write characteristics. Additionally, the proposed cell consumes 2.2× and 2.7× less static power compared to 6T cell and other 10T cells (10TCell-1, 10TCell-2 &10TCell-3).

3. Proposed cell

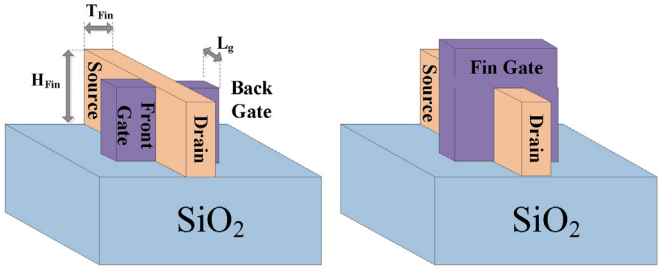
3.1. Cell functionality

The proposed SRAM cell is shown in Fig. 2. This structure consists of ten transistors with six main body transistors, similar to a conventional 6T cell. The four additional transistors are used to reduce the read path leakage, and to power-gate the cell in hold mode. Using separate paths for read and write operations improves the stability of the cell. The proposed cell has three operating modes: Read, Write and Hold modes. Throughout the paper, we refer to the read and write modes as *active* mode, and hold mode as *static* mode.

Table 1 shows the control signals to select different modes. The power gate transistor (M_G) is used at the bottom of the main body to switch the cell between active (read and write modes) and hold modes by changing the virtual ground voltage (VG). M_G is controlled by the HS (Hold-State) terminal. In active mode, the M_G transistor is turned ON by applying Vdd voltage to HS. Activating RWL or WWL signals enables read and write operations respectively.

3.2. Hold mode

Static Noise Margin (SNM) is defined as the maximum voltage noise that can be added to the output of each inverter (in main body of cell)



FinFET physical parameters

Gate Length, LG (nm)	24
Equivalent oxide thickness, EOT (nm)	1.1
Body Thickness, TFin (nm)	15
Height of Fin, HFin (nm)	28
Fin Pitch, FPitch (nm)	60
VDD (V)	0.8

Fig. 1. Structure of FinFET. (a) Independent-gate. (b) Common-gate devices.

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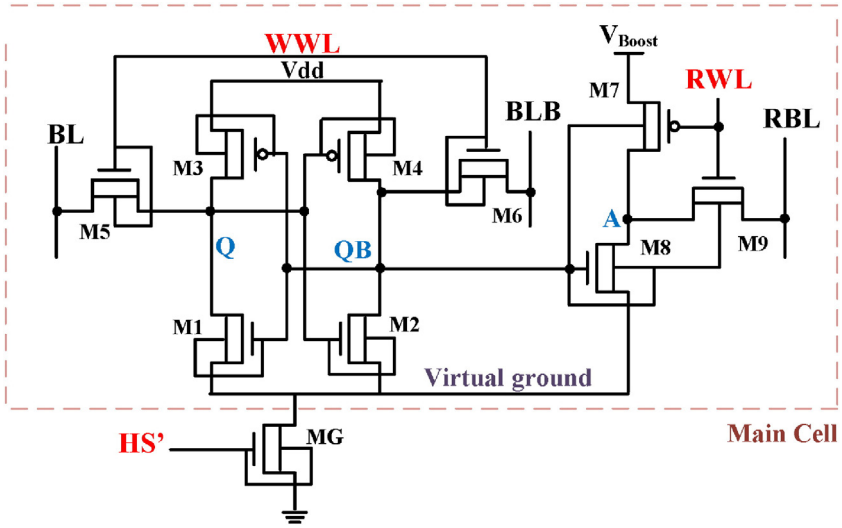

Fig. 2. Proposed 10T-SRAM cell structure.

such that cell works correctly. In the case of SRAM cell, SNM is defined as the length of the largest square that can be fitted inside the butterfly diagram of cell [22]. It is the most important figure-of-merit for SRAM cells that evaluates the stability of read, write and hold operations. Higher SNM in each mode results in better cell stability. Our proposed cell is designed such that it improves the cell stability in both read and hold modes with no major power and area overhead.

The M_G transistor acts as a power gating transistor which puts the cell into hold mode for reducing the static power consumption. In active mode, M_G is turned ON, and the effective voltage over the cell is slightly below Vdd due to the voltage drop over M_G. However, in hold mode, if zero voltage is applied to HS, M_G goes into weak state, allowing only the leakage current can pass through it. In this state, depending on the supply voltage, the data recovery (or retention) may become impossible due to the low hold stability. Instead, applying a non-zero voltage to HS terminal in hold mode improves the stability, albeit with the overhead of hold power consumption.

We experiment with different HS voltages considering both hold stability and power consumption. In hold mode, decreasing the HS signal (below Vdd), increases virtual GND (V_G) which results in lower effective voltage over the proposed cell. This significantly reduces leakage power by controlling the M_G and supply voltage current. As shown in Fig. 3, hold power has higher slope with respect to hold SNM in 300–500 mV. In ultra-low power systems, the HS signal can be set to 350 mV, which can increase power savings by 4.2× with respect to a baseline that assigns HS signal to Vdd. However, with this voltage the hold stability of cell decreases by 37%, which is not acceptable for sensitive and high variability systems. To maintain acceptable SNM, we select 400 mV as HS voltage in hold mode. At this design point, with just 24.2% hold SNM overhead, the hold power decreases by 2.2× respect to baseline. Repeating this procedure at near-threshold supply voltage shows that choosing 250 mV as HS signal allowed for 2.6× savings with 22.8% lower hold SNM. An advantage of adding M_G is that the virtual ground (Vx) goes up and reduces the effective voltage over the main body. This can improve write characteristics since writing in a weak cell is easier, i.e. it needs less time and energy. The other advantage of the design is the low sensitivity of cell parameters to HS signal variation, process variations, NBTI effect, etc. Since this signal only changes the tradeoff between hold power and hold SNM (see Fig. 3), a small variation on this voltage does not affect the cell performance.

Table 1
The control signals in different operation modes.

Cell modes	HS	WWL	RWL
Read	1	0	1
Write	1	1	0
Hold	0	0	0

3.3. Shared current concept

In this section, we compare the effect of utilizing shared tail transistor M_G as buffer of read path and main body in improving the cell stability in read and hold modes.

All recent cells with power gate transistor like [3,5,23], have access path connection to separate pair of transistors in the tail of the access path without any internal feedback (*isolated read path*). However, we make use of sharing the tail transistor for both the read paths and the cell main core to increase the cell stability by sharing their currents (*connected read path*). When M8 turns on, the current of the read path is added to the loop current in the tail transistor (M_G). The current stabilizes the operation of the cell during the read operation and thus increases the value of the read SNM considerably. Fig. 4 shows the current of M_G when the Q node voltage is swept from zero to nominal Vdd, for both connected and isolated read path. In the first case, the transistor current is high when the voltage of the Q node is zero. At this point, the QB voltage is high and this turns M8 ON and increases

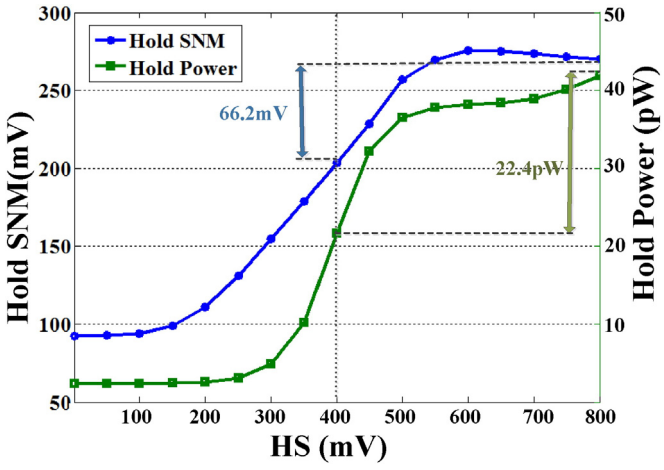

Fig. 3. Hold SNM and power tradeoff for HS signal with $(W/L)_{MG} = 1$.

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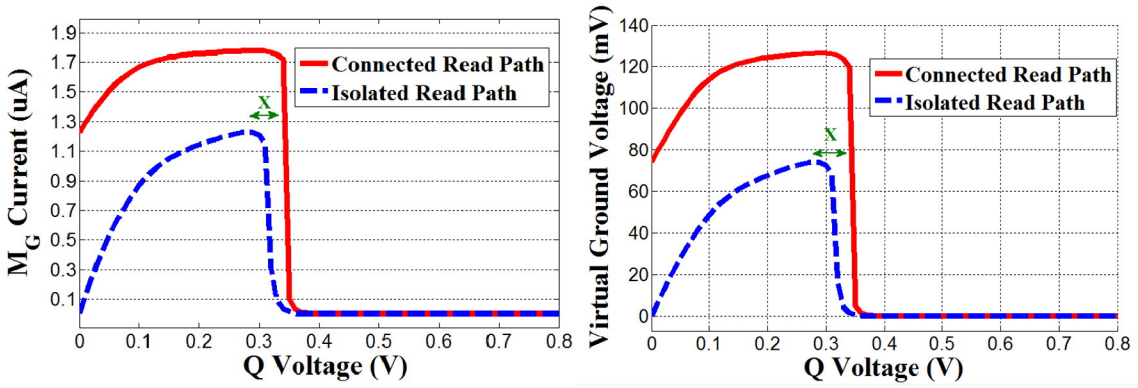

Fig. 4. The MG current and virtual ground voltage during swiping Q voltage.

the tail transistor current. In contrast, in the case of the isolated read path, this current passes through another transistor (not M_G) and just increases the static power of the cell. In both cases, the transistor current decreases as the voltage of the Q node becomes more than 350 mV where the cell value flips and the increase in the voltage beyond this value gives rise to the monotonic current increase in the connected read path case and zero current in the isolated read path case. Since the M_G is in linear region, the virtual ground voltage tracks the current through the tail transistor in the triode region. The virtual ground voltage becomes higher when the read paths are connected to the drain of the tail transistor when sweeping the voltage due to the current injection from the read paths.

As Fig. 4 suggests, for the connected read path case, QB is kept at high level for about the X interval (shown in Fig. 4) more than the isolated read path case because the read path currents are injected to the virtual ground node. Hence, the size of the fitted squared SNM inside the butterfly curves increases. This is a direct consequence of the dependency of the virtual ground voltage on the read path and the cell main core currents. Using this topology, the virtual ground voltage is dynamically changed depending on the current similarly to the current–voltage feedback for the tail transistor. The read path current can influence the virtual ground voltage, which is presented somehow in the QB node. This causes the QB node to have a higher voltage with respect to isolated read path topology, while the Q node voltage increases till the 350 mV. This affects the read SNM of the cell in such a way that the butterfly curves are more similar to squares in both sides as shown in Fig. 5. The value of SNM for the isolated read path is equal to 259 mV. Sharing the tail transistor causes the SNM to become equal to 276 mV.

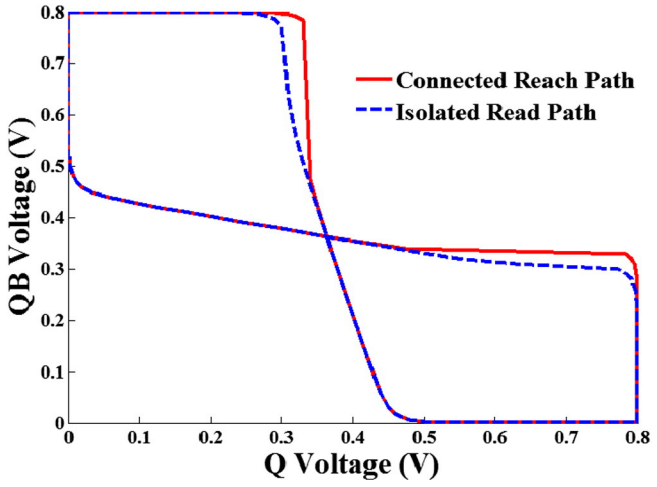

Fig. 5. Butterfly diagram for the read operation for isolated and connected read path.

The effectiveness of the feedback, or in other words, feedback gain (β) significantly depends on the size of the tail transistor and it can be studied for the optimization of the read SNM. The optimum size of the tail transistor depends on the level of supply voltage where the circuit works. To study the dependency, the read SNM versus the tail transistor (M_G) size for different supply voltages is depicted in Fig. 6. As the results show, the read SNM decreases by increasing the size of M_G for the supply voltages higher than 300 mV while in the 250 mV, the read SNM increases as M_G becomes larger. The behavior may be justified by considering the effect of the tail transistor on the SNM plot. When supply voltage is as low as 250 mV it cannot force the tail transistor to become fully ON in the read and write states. In other words, the virtual ground voltage becomes very high and lower portion of V_{dd} is applied over the cell. This reduces the voltage difference between the high and low levels of the logic circuit and disturbs the correct functioning of the cell. In this case, increasing the size of M_G reduces the tail transistor resistance and the virtual ground voltage improving the read SNM. While in the case of higher supply voltage, the tail transistor is effectively turned on when the supply voltage is applied to its gate. Increasing the size reduces the resistance, which weakens the feedback of the tail transistor in enlarging the read SNM. Therefore, for the higher supply voltages, a minimum number of fins should be considered based on layout design rules while at the supply voltage of 250 mV higher number of fins should be employed. Note that the effect of the tail transistors size on Hold SNM and read SNM is completely different because on hold mode there is no read path current to share with main body. Indeed, without share current concept the larger tail transistor results higher cell stability because the virtual ground is close to real ground. The main advantage of our design is to use this read current with no overhead in order to significantly improve the cell stability using sharing concept.

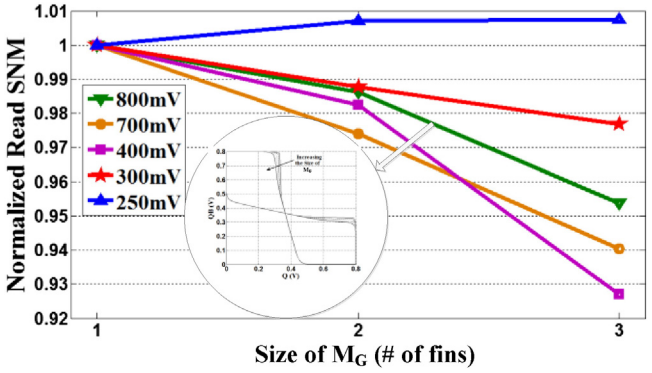

Fig. 6. Normalized read SNM versus the size of M_G for different levels of supply voltages (SNM has about 5% variation with respect to the size of M_G for the nominal supply voltage).

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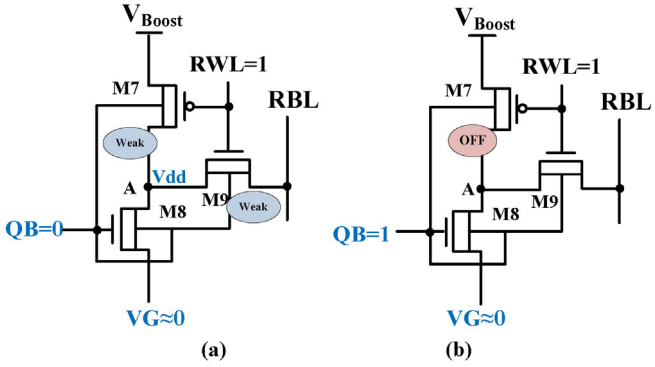

Fig. 7. Read operation of proposed architecture when (a) cell stores one (Q = 1) and (b) cell stores zero (Q = 0).

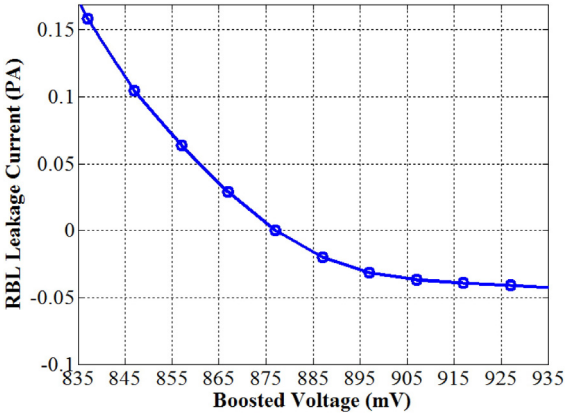

Fig. 9. RBL leakage current in different boosting.

3.4. ON/OFF read current ratio

Suppressing leakage current from the read bit line (RBL) and improving ON/OFF ratio is critical in sub-threshold and near-threshold regions. In a cache architecture, the read path leakage current through the cells may cause unwanted discharging of bitline, so the ON/OFF ratio limits the number of cells that can be connected to each bitline.

In the proposed cell, data is read from one side of the cell. In read operation, the cell is put in active mode (HS = 1) and RWL is set to one. When cell data is zero (Q = 0 and QB = 1), M8 and M9 transistors become active, discharging RBL through M_G tail transistor (see Fig. 7b). When the cell data is one (Q = 1 and QB = 0) the leakage current of read bitline decreases significantly due to (i) M9 weakness and (ii) Voltage Boosting. *M9 Weakness*: Connecting back gate of M9 to QB puts M9 in weak mode, which reduces the leakage current through RBL. Applying zero voltage to the back gate of M9 decreases gate-drain leakage current, which further reduces RBL leakage. *Voltage Boosting*: When reading one from the cell, M7 transistor becomes semi-active because the front and back gates of M7 are connected to RWL and QB voltages, which are one and zero respectively. As shown in Fig. 7a, this transistor charges node *A* and reduces the voltage drop across drain–source of M9. In the best case, node *A* voltage charges up to Vdd to create a zero voltage drop across M9. There is competition between M9 and M7 in setting node *A* voltage. To minimize the leakage current of M9 in this state, we use voltage boosting at the read path supply voltage (source voltage of M7 transistor). This voltage compensates for the weakness of M7 and ensures minimum leakage current in M9.

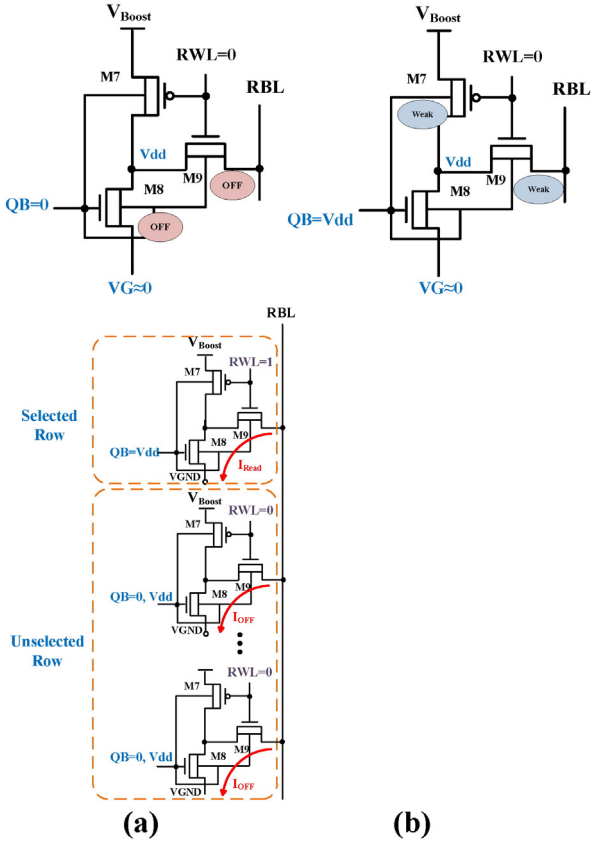

Fig. 8. Read path leakage current for unselected row during mode (a) cell stores one (QB = 0) and (b) cell stores zero (QB = 0).

During read mode, RWL signal in selected row is one and the rest unselected rows in same column bias with RWL = 0 (Fig. 8). The ON current defines for selected cell when QB = 1 while the OFF current defines as leakage current through RBL when the cell is not in read mode (RWL = 0). The worst-case scenario is when QB = 1 for unselected cells (RWL = 0) and QB = 0 for selected cell in same column. In this condition, the leakage current through RBL is maximized but the array should be robust to cell's leakage and doesn't consider summation of leakage currents as ON current. Here we show that the proposed cell has extremely low RBL leakage current either with QB = 1 or QB = 0. Fig. 8 shows two read OFF current scenarios. When the cell data is one (Q = 1, QB = 0), M8 and M9 suppress leakage through the read bit line. When the cell save one, M9 transistor is semi-active but its leakage is controlled by M7 transistor since node *A* is charged to Vdd voltage through the voltage boosting method. In both scenarios, we have Vdd voltage on node *A*, which significantly suppresses OFF current of unselected cells in same column (same RBL). In addition, power gating (using M_G) reduces the effective voltage of all intermediate nodes, decreasing the overall leakage current.

The RBL leakage current at different boost voltages for 800 mV nominal Vdd is plotted in Fig. 9. As figure shows, selecting V_{Boost} close to 870 mV charges node *A* to the desired value and minimizes RBL leakage current. Choosing V_{Boost} higher than 870 mV inverts the direction of M9 current and current inject to the RBL (negative current). The same

Table 2
RBL leakage current reduction by employing voltage boosting.

Supply voltage	ΔV_{Boost}	RBL leakage current (pA)	
		Without V_{Boost}	With V_{Boost}
0.2	20 mV	468.59	1.34
0.3	35 mV	541.84	0.505
0.5	50 mV	575.63	0.103
0.7	65 mV	5.59	0.056
0.8	70 mV	0.65	0.031

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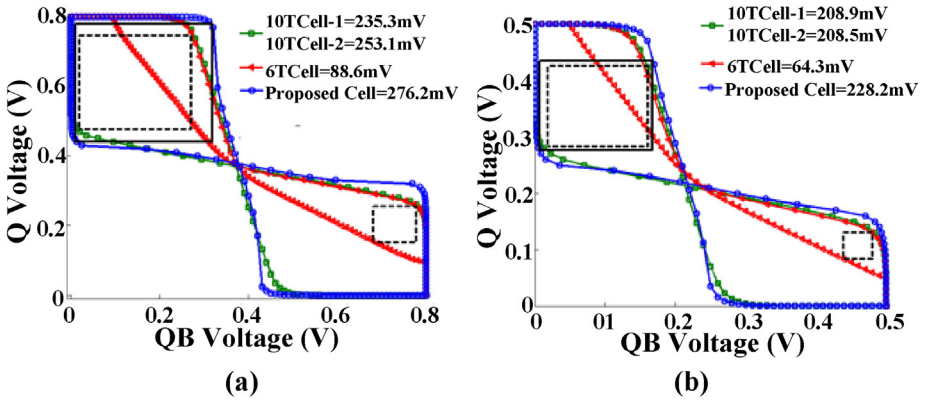

Fig. 10. Butterfly diagram for read operation in (a) above threshold and (b) near threshold regions with $(W/L)_{MG} = 1$ and HS = V_{dd}.

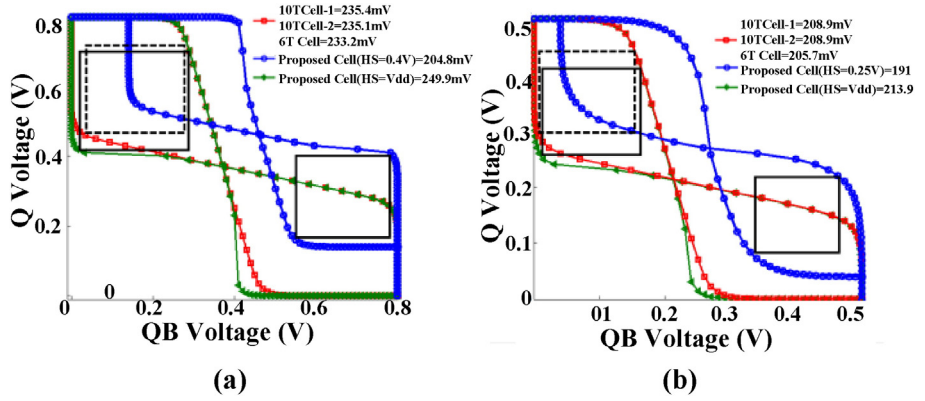

Fig. 11. Butterfly diagram for Hold operation in (a) above threshold (HS = 400 mV) and (b) near threshold (HS = 250 mV) regions with $(W/L)_{MG} = 1$.

procedure is followed with different supply voltages to find the best value of V_{Boost}. The effect of voltage boosting on read path leakage current is shown in Table 2. With $V_{Boost} = 800$ mV supply voltage, 20× lower leakage current is observed through RBL than $V_{Boost} = 200$ mV.

In SRAM cells, the read power consists of three components as Eq. (1). First, the require power to charge the RWL during the read mode. The power consumption of pre-charging and discharging of for RBL and the third element is the power overhead of the voltage boosting.

$$P_{\text{Read}} = \Delta P_{RWL} + \Delta P_{RBL} + \Delta_{Boost} \tag{1}$$

In SRAM array the read power can be expressed generally as:

$$P_{\text{Read}} = N_{RWL} C_{RBL} \Delta V_{RBL} V_{dd} f + N_{RBL} C_{RWL} V_{dd}^2 f + N_{RWL} C_{Boost} \Delta V_{Boost} V_{dd} f \tag{2}$$

In this equation the difference is in third term ΔP_{Boost} where in other method this term replaced with$\Delta P_{norm-Vdd}$. Based on Table 2, voltage boosting just added less than <70 mV to Vdd in all supply voltage. Therefore, this term can increase the read power at worse case by 5%. Note that the read power is not important factor in total SRAM power since the static power is the main source of power consumption on today's SRAM chips. We used boost circuit on [24] that used a single circuit with negligible area and static power respect to high Leakey SRAM cell. More details about implemented voltage boosting is explained at [24,25].

3.5. Loop leakage current reduction

In hold mode, RBL is not pre-charged in order to eliminate leakage. Loop leakage current can occur between the internal nodes of different cells connected to the same bit line through RBL. This current can affect the charge on internal nodes and sometimes create a short circuit. This is an issue in cells with high leakage current from read bitline, which affects the stability of the internal node. For example when 10TCell-2 is not in read mode, the source of read access transistor is not fixed and instead depends on stored data on cell (drain–source voltage are changing). Typically, a cache structure consists of several cells that share RBL. The different voltages of this node in these cells can increase leakage through read path transistors and produce loop current among intermediate nodes. To address this problem, we need voltage at the source of read access transistor to be independent of the stored value in a cell. In proposed cell, the tail transistor not only reduces the leakage of the main memory in hold mode but also suppresses the read path leakage current and control loop current. In this mode, the M_G transistor is OFF (weak) so the read path is buffered at least by the tail transistor.

Table 3
The ON current (uA) and OFF current (fA) through RBL in different supply voltages.

Vdd	10TCell-3		10TCell-2		10TCell-1		Proposed cell	
	ON	OFF	ON	OFF	ON	OFF	ON	OFF
0.2 V	0.9	8486	0.5	6570	0.5	1230	0.5	1340
0.3 V	9.3	1636.4	5.4	1240	5.4	1.5e4	5.4	505.6
0.5 V	56.9	975.4	31.9	680.4	31.9	2.3e4	31.9	103.9
0.7 V	124.6	1168.3	68.0	796.1	68.0	3.6e4	68.0	56.7
0.8 V	161.1	1295.6	87.2	884.3	87.2	4.4e4	87.2	31.5

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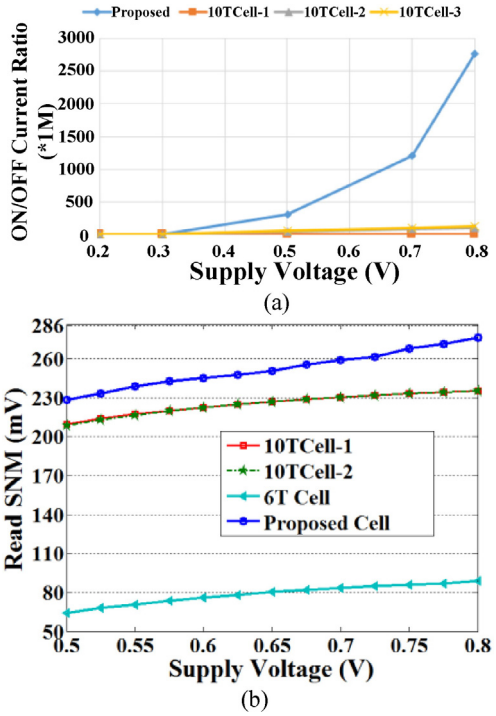

Fig. 12. Read characteristics of cells (a) ON/OFF current ratio and (b) Read SNM in different supply voltages with $(W/L)_{MG} = 1$.

4. Results

In this section, we compare the proposed SRAM cell to conventional 6T and three low power and stable SRAM cells from literature (10TCell-1, 10TCell-2 and 10TCell-3). Our goal is to evaluate the ability of proposed cell to decrease the read path leakage, hold power and cell variations with respect to other state-of-the-art cells. We compare cell characteristics of read and hold SNM, write access time, read current, power consumption and variation. For fair comparison, all structures are designed with 20 nm independent gate FinFET (IGFinFET) [9]. The simulations are performed using HSPICE tool. The results are obtained at two different supply voltages, 800 mV and 500 mV, which are respectively above and near threshold voltages in this technology. During active mode, HS signal is set to Vdd voltage, however in hold mode this signal is biased respectively by 400 mV and 250 mV in above and near threshold regions, as discussed in Section 3.2. All cells are simulated in standard size where number of fins in PFET and NFETs in main body (access transistors) are 1 and 2 (1 and 1.5) respectively. The results of proposed cell are compared to 10TCell-1 [2] and 10TCell-2 [16]. Since 10TCell-3 and 10TCell-2 are similar structures that differ only in read characteristics (i.e. ON and OFF current), we only show the results for 10TCell-3 in Section 4.2.

4.1. SNM

Fig. 10 compares the butterfly diagrams of read operation for proposed cell, 6T, 10T-Cell-1 and 10TCell-2 in above and nearthreshold regions. The proposed cell shows at least 17.4% and 9.2% higher read SNM compared to other structures at above and nearthreshold supply voltage respectively. The hold SNM of the proposed architecture at two different HS signals is also computed. For hold mode, we apply 400 mV and 250 mV to HS at above-threshold and near threshold respectively. Gating the cell reduces the hold SNM. However, due to the high stability of cell in this mode, this reduction is negligible. With HS biased to 400 mV and 250 mV in above and nearthreshold regions, the hold SNM in the worst case is about 31 mV (13.1%) and 18 mV (8.4%) lower than the best SNM value of other structures. Given its significant power reduction, this SNM can be acceptable in many applications since the SRAM cells typically suffer from failure in read/write mode, while they are inactive and stable in hold mode [26] (Fig. 11).

4.2. Read characteristics

In subthreshold and near threshold SRAM cells, the read current is an important characteristic which determines the speed of cells. This current affects the time required for reading the cell and discharging the bitlines. Read leakage current is important because ON/OFF current ratio determines the maximum number of cells that can be connected in parallel within each column of a memory array. The proposed cell employs novel back-gate connections on access transistors and voltage boosting to reduce the RBL leakage current. Note that we do not show results for 6T cell here, since 10T structures are radically different, and are proposed to particularly address read stability issues in 6T cell.

The ON and OFF currents through RBL at different supply voltages for 1 K cell per bitline are listed in Table 3. We show a wider range of supply voltage to cover subthreshold, nearthreshold and above threshold regions. All three 10T cells in literature have strong read characteristics at low supply voltages. The results show that the proposed cell has extremely low leakage currents with respect to other cells at all supply voltages. Except 10TCell-3, the other cells have comparable ON current. Although 10TCell-3 has higher ON current (due to usage of two parallel transistors in read path), it has high and unacceptable OFF current. As shown in Table 5, the OFF current of all cells except 10TCell1 increases as supply voltage is reduced. In OFF state, 10TCell-1 does not employ intermediate nodes to reduce drain–source current of read access transistor. Thus, the effective voltage over the access transistor is close to Vdd. As a result, higher supply voltage results in higher OFF current. Other 10T cells use a P-type FinFET (PFET) transistor to charge the source voltage of read access transistor and set drain–source of access transistor to

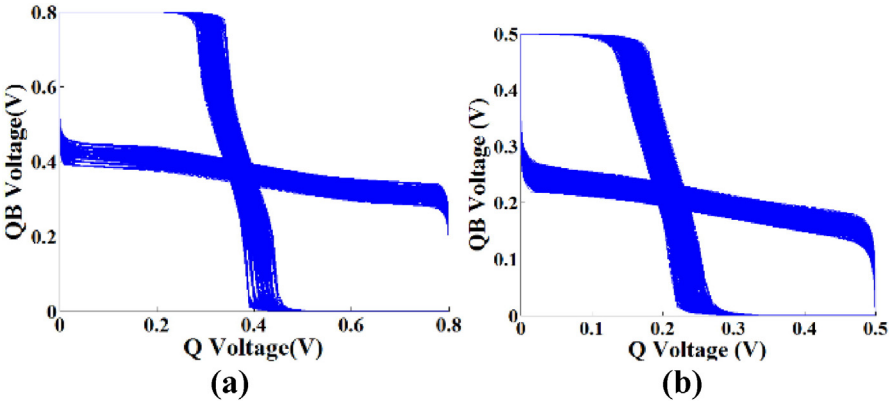

Fig. 13. The read butterfly diagrams of the proposed cell at (a) above threshold (b) near threshold region with HS = Vdd.

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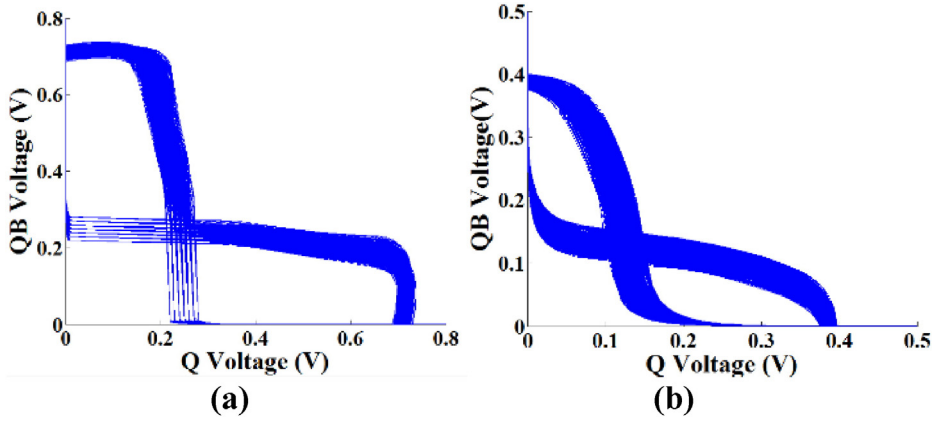

Fig. 14. The hold butterfly diagrams of the proposed cell at (a) above threshold and (b) near threshold region.

zero (similar to the role of M7 in proposed cell). However, at lower supply voltage, due to the weakness of the PFET transistor, the drain–source voltage across access transistor increases, causing higher OFF current.

Fig. 12a compares the ON/OFF current ratio of proposed cell and other cells at different supply voltages. Improvement of ON/OFF current in proposed cell is significant at higher supply voltages. The results show that the proposed structure has at least 20× and 6.5× higher ON/OFF current with respect to other cells in above and near-threshold regions. In the proposed cell, the RBL access transistor is in weak mode, which can effectively reduce the leakage current through it. Further, at each supply voltage we set V_{Boost} to appropriate voltage such that the leakage current through RBL is minimal. Fig. 12b shows read SNM variation versus supply voltage. The proposed structure has better stability in read mode compared to other structures. In the proposed cell, the tail transistor reshapes the butterfly diagram. This improvement is useful specifically at lower supply voltages such as near-threshold voltage region. SRAM cells with the same main body structures have similar SNM. The slight difference between structures comes from the buffering of read path, which reduces the leakage current by stacking effect.

4.3. Power and process variations

For each transistor, we consider variation in both, threshold voltage and transistor size. The variation is modeled as Gaussian distribution with 3σ equal to 10% of the original value [27]. The read and hold butterfly diagrams, considering 5000 Monte Carlo simulations, are demonstrated in Figs. 13 and 14. The comparison of the SNM variation shows that the proposed cell can significantly suppress the effect of process variations in SNM. This is due to the use of power gate transistor, which acts as an inner feedback for the system. When the current passing through the tail transistor increases, the virtual ground goes up proportionally, so that the effective voltage over the cell reduces. This can adaptively control the effect of transistor variations on cell. The values of STD to mean for read and hold SNM in different structures are demonstrated in Table 4. As shown, the resultant feedback can suppress SNM variation such that it improves read SNM (hold SNM) by at least 17.4% and 12.4% (8.9% and 10.3%) compared to other structures at near threshold and above threshold respectively.

Total power consumption of SRAM cells can be broken down into static and dynamic power. The 10T cells and the proposed cell consume similar write power since they employ the same transistor structure as the 6T cell for write operation. As discussed in Section 4.2, the proposed cell has comparable read power with respect to other 10T cells. Thus, the dynamic power of proposed cells is comparable with other 10T cells in literature. Static power is already a significant part of power consumption in SRAM cells [28]. The relative contribution of static power to the total SRAM power is expected to further increase in future because of the exponential relation of leakage currents with technology scaling [29]. The memory cells are not active in hold mode, so the hold power represents majority of the static power of SRAM cells.

The static power and its variation in near threshold and above threshold regions with Monte Carlo simulation is demonstrated in Table 5. In above threshold region (near threshold region), the proposed structure has at least 2.2× and 2.7× (2.6× and 3.5×) lower static power with 23% and 15% (15% and 16%) lower static power variation respect to 6T and other 10T cells respectively. In the proposed cell, M_G acts as internal feedback, controlling the variability of cell. Supply voltage current passes through M_G transistor. As this transistor is in linear mode, the current is proportional to the voltage drop across this transistor. Due to variation, if the cell current increases (decreases), the M_G current and resulting virtual GND voltage increases (decreases). This reduces the effective supply voltage over the cell and reduces M_G current (adaptive internal feedback). Thus, the power gating transistor acts as resistive feedback and suppresses the variation of the cell.

4.4. Write characteristics

One of the main issue of write operation in all SRAM cells is that the bitlines are not strong enough to write their value due to the competition of access transistors and pull-down transistors in the main body. The proposed structure uses a tail transistor (M_G), which weakens the back to back inverter in active mode, and improves write ability. Writing

Table 4
Read and hold SNMs and their variations (STD/Mean) in near and above threshold supply voltages.

Structures	RSNM variation (%)		HSNM variation (%)	
	Near threshold	Above threshold	Near threshold	Above threshold
6TCell	5.13	4.63	9.14	7.78
10TCell-1	3.97	2.42	6.49	5.26
10TCell-2	3.73	2.26	6.38	4.97
Proposed cell	2.98	1.74	5.63	4.27

Table 5
Static power (hold power) consumption and its variation (STD/Mean) at above and near threshold voltages.

Structures	Above threshold		Near threshold	
	Power (pW)	Variation (%)	Power (pW)	Variation (%)
6TCell	44.7	6.93	0.91	5.28
10TCell-1	55.2	6.28	1.17	5.34
10TCell-2	83.2	7.50	1.41	6.03
Proposed cell	20.3	5.32	0.33	4.49

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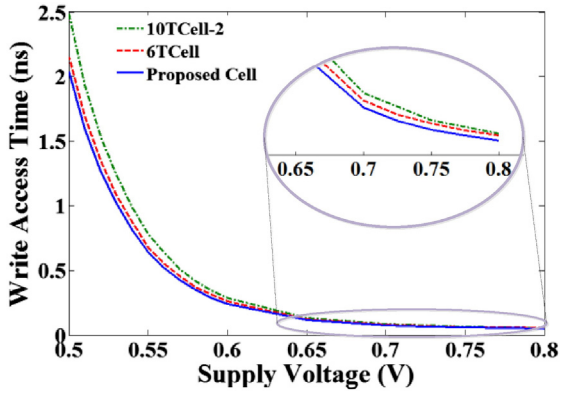

Fig. 15. Write access time in different supply voltages with $(W/L)_{MG} = 1$.

in a weak back-to-back inverter is easier since values can be switched faster.

The comparison of write characteristics of proposed cell versus other structures is demonstrated in Fig. 15. The results show that the write access time is 7.2% and 5.6% faster than 10T cells and 6T with 800 mV supply voltage. This improvement decreases to 4.4% and 1.7% with 500 mV supply voltage with respect to 10T cells and 6T.

4.5. Area

The improved read, write and hold characteristics of the proposed cell seek to address the process variation, stability and power challenges of the 6T cell. This improvement comes at the expense of about 30% higher area. The layout in Fig. 16 shows that the area of the proposed cell is 330 nm*472 nm. Similar to other 10T cells, the proposed cell physically has ten transistors in its structure, with the difference that its tail transistor can be shared between cells in each row or block (therefore, the effective number of transistors in the proposed cell is nine). The comparison of the proposed cell layout with other 10T cells [2,16,17] shows that our cell is smaller than other 10T cells due to sharing of back-gates between read transistors. This, along with sharing of tail transistor makes the layout simpler. The area of the cell can be further shrunk since the high ON/OFF current ratio in proposed cell helps us to add more cells in the same column, which results in sharing peripherals used for each column. Other strategy to improve the area efficiency is using IG-FinFET just in the read path transistors (M7–M9) and utilizing CG-FinFET for the rest of transistors (M1–M6, MG). This hybrid usage of FinFET improves SRAM array density respect to pure IG-FinFET based SRAM design.

5. Conclusion

This paper introduces new technique to design ultra-low leakage SRAM cell which improves cell characteristics in read, write and hold modes in 20 nm in independent gate FinFET technology. The usage of FinFET back gates and boosting of the supply voltage of read path improves ON/OFF ratio by at least 20× and 6.5× over prior cell designs in above and near threshold regions. Utilizing a power gate transistor in the tail of the storage cell and sharing read path and main body current, reduces the hold power, reshapes the butterfly diagram (higher read SNM stability) and acts as internal feedback to adaptively suppress the variability of the cell. In addition, this decreases the voltage drop over the cell in write and hold modes, improving write ability and significantly reducing the static power of cell. In above threshold (near threshold) region, the proposed structure has at least 2.2× and 2.7× (2.6× and 3.5×) lower static power with 23% and 15% (15% and 16%) lower static power variation with respect to 6T and other state-of-the-art 10T cells.

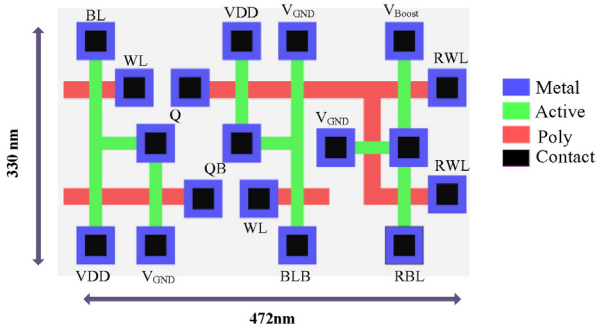

Fig. 16. Layout of proposed 10T cell.

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